

Signal and Image Processing Via Reconfigurable Computing

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Abstract *Modern signal processing is now critically dependent on timely data processing. Signal and image processing algorithms will face challenge in applications because of their intensive computation. This paper reviews the general signal processing implementation platform and the problems that typical signal/image processing algorithms might have when applied in real time application. The functionality of reconfigurable computing techniques in speeding up signal/image processing algorithms is accessed. Design examples from literatures are presented as well. The importance of reconfigurable computing technology in modern signal and image processing is analyzed and emphasized.*

Keywords: signal processing, reconfigurable computing, FPGA, real-time applications, performance

1. Introduction

Digital Signal Processing (DSP) technologies have found great applications in a variety of areas including audio, video, speech and communications. DSP algorithms are ideal for hardware implementation because of their inherent data parallelism and the common computational units found in most signal processing functions. The potential of DSP theory has been expanded when combined with powerful computation tools. With the profound research in information technology and wireless communications, the demand for high-performance and computational intensive implementations is increased.

Generally, performance and flexibility are two goals that must be met when a hardware implementation platform is chosen for a digital signal processing system. Most application specific integrated circuits (ASIC) have high performance and relatively low cost, but are lack of flexibility. Digital signal processors and general microprocessors present high programmability while their performance is limited. Reconfigurable machines offer a good compromise between performance and flexibility and have attracted highly attentions from researchers.

Reconfigurable computing for DSP remains an active research area as the need for integration of complex DSP algorithms is intensified.

This paper reviews the challenges that typical signal/image processing algorithms might face in real-time applications, and the functionality of reconfigurable computing techniques in speeding up signal/image processing algorithms. The rest of the paper is organized as follows. Section 2 reviews four DSP implementation platforms. Their features for real-time signal processing applications are compared and analyzed. Field Programmable Gate Arrays (FPGA) and their functionality of speeding up DSP applications are discussed in Section 3. Typical DSP applications that can take advantage of reconfigurable computing are presented in Section 4 followed by two case studies in Section 5. Future direction in signal processing via reconfigurable computing is analyzed in Section 6.

2. Review of DSP implementations

2.1 DSP application platforms

Implementing algorithms on hardware platforms is an essential step in signal processing technology. Research is not complete if an algorithm is not feasible to be implemented or hardware architecture is not available. Generally, performance and flexibility are two goals that must be met when a hardware implementation platform is chosen for a digital signal processing system. A good hardware platform should provide good performance including high computation throughput, low power consumption, and small design area. It should also be easy to program and flexible to change. The results of these cost tradeoffs have resulted in four implementation solutions that include application-specific integrated circuits (ASIC), digital signal processor (DSP), general-purpose microprocessors (microp), and reconfigurable hardware (FPGA) [1]. The strength and weakness of each architecture are compared in Table 1.

	Flexibility		Performance		
	Programmability	Reconfigurability	Area Utilization	Power consumption	Computational throughput
ASIC	Low	low	low	low	high
DSP	medium	medium	high	high	low
Microp	medium	high	high	high	low
FPGA	medium	high	low	medium	medium

Table 1 Signal processing implementation platform comparison [1][2]

ASIC provides high performance in terms of area, power consumption and throughput. But as the name indicated, ASIC is application specific and it is only good for certain applications. If a design changes, for example, a FIR filter needs more taps, another ASIC has to be employed or designed. Design ASIC is an expensive task considering of its long development cycle and manpower. In addition, ASIC design is generally implemented using hardware description language (HDL), that is not easy to implement complicated algorithms, and even a square root function needs a few lines of code to find approximation or table look up.

Digital signal processor is generally single-stream instruction set processors optimized for high-speed arithmetic, especially for typical multiply and accumulation (MAC) function [3]. Implementing designs using high-level language C or C++, DSP platform is programmer-friendly. The problem for DSP processor is its low data throughput and less resource efficiency. High-level compiler is often difficult to optimally use the design resource. The memory access speed might be a bottleneck for gigabyte data transfer. Additionally, DSP chip is sequential, and it does not support parallelism.

General-purpose microprocessor or microcontroller is single stream instruction set optimized for message-passing. It is feasible for some applications such as changing the number of taps in an FIR filter, but the big drawback for microprocessor is its less efficiency in terms of using recourses.

Reconfigurable computing platform offers a good intermediate solution for DSP applications considering its rich resources, fast configuration speed, reconfigurability and support for parallelism. Its rich resources support the implementation of more complicated algorithms like Viterbi decoder or wavelet-based data compression. The parallelism ensures the possibility of high-performance using FPGA without distributing arithmetic [3]. Its fast configuration speed and reconfigurability make it possible to repeatedly program the device resource working with different functions at different time, therefore decreasing the system cost and improving the performance. For example, when a neural network is implemented on an FPGA, weights stored at on-chip RAM can be updated at run-time during the training stage. The same recourse can be configured for

working function when the training converges and the weights can be read from the same location. System performance increases because of avoiding transferring data (weights) from one location to another, and the system cost is decreased because the same resource is used to performance two different functions.

2.2 Challenges in real-time implementation

Emerging reconfigurable technology with signal processing algorithm becomes crucial for modern DSP applications. Even traditional signal processing algorithms will face challenge when they are applied for high data rate applications. Dunham [4] reinforced the importance of reconfigurable computing when applying matched filter detection for image sensor data processing. In this application, multiple matched filters need to be convolved at same time and 10 Giga-operations per second is required to ensure the system performance. Reconfigurable computing system provides ultimate solution for timely data processing in this application because of its fast speed and parallelism.

Image processing requirements and the advantages of FPGA for image processing have been analyzed in [5]. This paper indicated that a good image processing platform should be able to process large images with more than 10,000 by 10,000 pixels and should have high computing performance during local calculation avoiding transmitting large amount of data between host and clients. The ability of computing with different word size for varying pixel precisions is another issue needs to be considered because some images have pixels with twelve or more bits of information, while others have only eight or four bits information. The author pointed out that Large-scale yet flexible fine-grained parallelism, operations with variable data size, and the integration of storage and computation within a single FPGA unit are keys that make reconfigurable computing system potential for image processing.

3. Introduction of reconfigurable computing

The core processor of reconfigurable computing machine is Field programmable Gate Arrays (FPGAs). Invented by Xilinx Inc in 1984[6], FPGAs have been the

subject of extensive research and experimentation. This section briefly reviews the architecture of FPGA and its functionality that is suitable for DSP applications.

3.1 Field Programmable Gate Arrays

FPGAs are generic, programmable digital devices that can perform complex logical operations. It is consisted of programmable logic blocks and interconnected wires and switches. Figure 1 shows a typical FPGA architecture. Logic functionality for each block is specified via a small programmable memory, called a *lookup table*. Additionally, each logic block typically contains one or more flip flops for storage. Wires and switches around logic blocks are configured to connect the resources that have been specified inside the logic blocks. Both of the logic blocks and wires are software programmable. One can repeatedly configure these resources at run-time or configure part of the resource to achieve lower hardware cost.

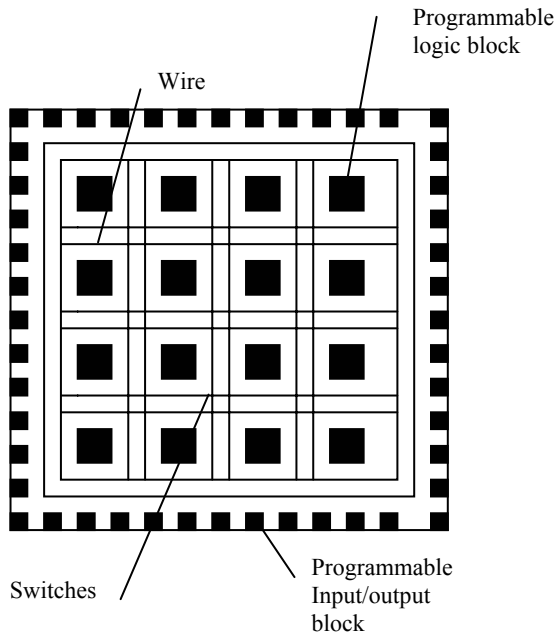


Figure 1 A typical FPGA architecture

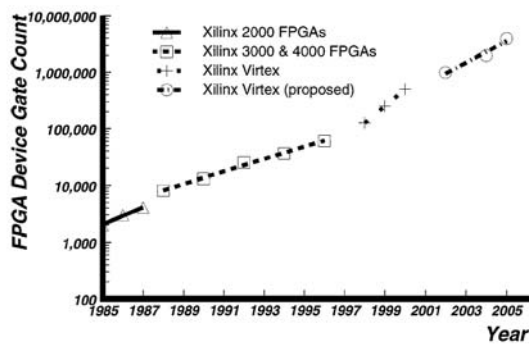


Figure 2 Growth of FPGA capacities [1]

Research in reconfigurable computing has been stimulated with the development and maturation of FPGAs. As shown in Figure 2, gate capacity for LUT-based FPGAs has been increased dramatically on the past years, which provide rich resources to implement more complicated algorithms.

To promote reconfiguration at low cost and fast speed, extensive research has been conducted in FPGA Computer Aided Design (CAD) tools [7][8] to ensure high-level compilation and efficient design cycles. FPGAs can replace thousands or millions of logic gates in multilevel structures. Their high density of logic gates and routing resources, and their fast reconfiguration speed give them the advantage of being extremely powerful for many applications. FPGAs are widely used because of their rich resources, configurable abilities and low development risk, making them increasingly popular.

3.2 Reconfigurable computing for DSP

Research about employing DSP algorithms and reconfigurable computing has been continued for almost two decades. Their inherent data parallelism and the common computational units found in most signal processing functions make reconfigurable computer the ideal platform for DSP algorithms. Tessier and Burleson summarized the direct benefits of the reconfigurable approach for DSP in three critical areas: functional specialization, platform reconfigurability, and the fine-grained parallelism [1]. The FPGA devices can be easily programmed to customize a specific application, even for some irregular data path and constraints. Taking advantage of the configurability and reconfigurability, pre-defined applications with varying number of parameters can be stored in on-chip Memory and loaded on the FPGA device if changes are made in the design. For example, for FIR filters, the coefficients of different filters can be stored in different locations of the RAM, and loaded on the device when necessary. Several filters can be implemented without re-compilation in general digital signal processor. The fine-grained parallelism found in configurable devices makes them well-suited for implementations including image processing, video and audio signal processing.

4. Applications in Signal/Image processing

After reviewing the FPGA architecture and its functionality for DSP implementation, this section reviews the typical DSP applications that can be mapped to FPGA devices.

Image Processing

Image processing applications generally involve simple operations applied to large images. For example, it is typical to perform edge detection operations or cross-correlations to an image. Both vector or pipeline processor and FPGA devices can perform the function taking

advantage of the implicit parallelism, reconfigurable computing outperforms the single instruction multiple data (SIMD) system because they are more efficient to handle problems including large data rate, varying data accuracy, multiple data access patterns like FFT, and multiple runtime environments [5]. Coric [9] presented an innovative application via optimizing an FPGA implementation for medical imaging. A parallel-beam backprojection algorithm used in CT has been implemented in FPGA concentrating on minimizing error while maximizing efficiency. This implementation has shown significant speedup over software versions of the same algorithm, and is more flexible than an ASIC implementation. Athanas and Abbott [10] worked on real-time image processing on a custom computing platform. Tasks such as Gaussian pyramid-based image compression, image filtering with 1D and 2D transforms, and image conversion using DFT operations were discussed.

Video Processing

Similar as image processing, high data bandwidth is the concern in video signal processing. Reconfigurable computing platform has been adapted to video processing to meet the requirement of high data capacity. The PAM system [11] was the first platform used in video applications. An FPGA architecture for video encoding according to the H.263 standard for video teleconferencing system was presented in [12]. Other interesting applications of FPGAs for video applications using single or multiple devices can be found in [13][14].

Audio and Speech Processing

Reconfigurable computing benefits audio and speech processing in datapath specification and pipelining [11]. Applications in this area can be found in nonlinear distortion [15], dynamical audio player, and echo cancellation [16].

Coding and Wireless Communications

Coding scheme has played an important role to improve signal-to-noise ratio in modern communication system. Several reconfigurable computing systems have been implemented for popular coding schemes including convolutional coding and Viterbi detector. A run-length Viterbi decoder can achieve 1 Mbits decode rate as reported in [17].

Software defined radio is another good application of reconfigurable system. Reconfigurability is crucial in wireless system components to support a range of standards. Cummings described how FPGA technology's unique combination of size and power efficiency plus field programmability offers a transition of FPGA from ASIC prototyping to embedded products [3]. A unified architecture, named as the layered Radio Architecture, for design of soft radio in a reconfigurable platform has been

presented in [18]. In the future, FPGA flexibility and high performance will find wider applications in wireless communications such as modulation, demodulation and fast Fourier transform [3].

Target tracking and recognition

Another important application is target recognition. Targets are detected via broking images into columns [19] or pieces [20] and dynamically swapping target templates. FPGA provides the unique functionality to customize templates to meet the detailed requirement for different target technology, which is not possible for application specific circuits. FPGAs were also used for real-time stereo as part of a face detection/tracking system embedded in an entertainment application [21].

5. Case study

This section studies two design examples to explain how reconfigurable computing technology could help signal processing algorithms improve performance in real application.

Case 1: A dynamically reconfigurable adaptive Viterbi Decoder

This paragraph reviews an FPGA implementation of an adaptive Viterbi Decoder presented in [22]. Error correct coding is widely employed in wireless communications to overcome data corruption. Convolutional code and its decoder, Viterbi decoder, are popular in various wireless standards. This work described the analysis and implementation of an Adaptive Viterbi Algorithm (AVA) in reconfigurable hardware. The adaptive Viterbi algorithm was employed to reduce the average computation and path storage required by the Viterbi algorithm [23]. The AVA implementation is targeted to a Xilinx XC4036XL FPGA to take advantage of computational specialization and parallelism. Reconfigurability of FPGA benefits the system to achieve constant bit-error rate. If channel noise increases, a more accurate decoder is loaded into the FPGA hardware. The performance of this reconfigurable implementation is compared with that in microprocessor and Digital Signal Processor. This FPGA implementation achieves a 7.5X speed up than that on a 366MHz Intel Celeron processor with 128MB of memory, and is about 29 times faster when compared with a 200 MHz TMS320C6201 DSP processor. Their experimental results indicated that dynamic reconfiguration can be used effectively to improve overall performance by at least 20%. This research work is a good example showing the functionality of reconfigurable computing in improving the system performance.

Case 2: Reconfigurable FPGA for real time image processing space

The implementation of image processing algorithms and techniques on FPGAs for space application were discussed

in [24]. Image processing is frequently used in remote sensor applications. The high data rate brings intensive computation on image analysis and introduces significant delays between image capture and analysis. Implementing image processing algorithms on reconfigurable system provides real time or near real time image processing for space applications, therefore enabling the technology for future generations of smart remote sensor system[24][25]. This research presented the implementation, testing, and performance evaluation of a Gaussian filter and Convolution Engine on High-Performance Computing (HPC –I) payload. Gaussian filtering is a fundamental operator in image processing at the aim of reducing the effect of random noise in images. Implementing Gaussian filter on FPGA platform provides more flexibilities of the design. The filter can be made adaptive via changing the size, or the values of the filter coefficients. These changes are useful when processing pixels at different locations of an image. Images at the edge and the center may need different filtering matrix. The system can be parameterized to processing arbitrary image size taking advantage of the reconfigurability of FPGAs. The performance evaluation in this research work indicated that FPGA offers the potential for enormous processing rates when employed in pixel-pipeline architecture.

6. Future Directions

Reconfigurable computing is a promising technology for implementations of future signal processing techniques. Research work will continuously concentrate on general rules of mapping algorithms to FPGA so that each application can optimally take advantages of FPGA resources. Design tools play an essential role in FPGA application. Requirement of mature and robust computer-aided design tools and high efficient compiler will remain constant, and research in this area will attract more attentions. With the development of silicon technology, the performance of DSP processor will be improved. How to partition a computational task to FPGA and DSP, and how to combining the strong points of both FPGA and DSP are also interesting topics in the near future. In conclusion, with the support of the powerful reconfigurable computing technologies, signal processing techniques will continuously find great applications in a variety of area.

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Dr. Jing Ma's research interests concentrate on reconfigurable computing applications in signal and image processing, reconfigurable architecture, and computer-aided design tools and algorithms for large-scale FPGAs. Related experiences include reconfigurable wavelet core implementation, reconfigurable mp3 players, and digital predistortion techniques using FPGA. Dr. Ma is seeking collaboration opportunities among committee members.